11.2. In the amplifier of Fig. 11.61, $R_D = 1 \, \text{k}\Omega$ and $C_L = 1 \, \text{pF}$. Neglecting channel-length modulation and other capacitances, determine the frequency at which the gain falls by 10% ($\approx 1 \, \text{dB}$).

![Figure 11.61]

\[
V_{\text{in}} = -\frac{q_m}{R_1} \frac{1}{C_s} \Rightarrow \frac{V_{\text{in}}}{V_{\text{S}}} = -\frac{q_m}{R_1} \frac{1}{C_s}
\]

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{q_m}{R_1} \frac{1}{C_s + 1} \Rightarrow \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{q_m}{R_1} \frac{1}{C_s + 1}
\]

\[
\Rightarrow \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{q_m R_1}{\sqrt{1 + (2q_m R_1 C_s)}}
\]

\[
20 \log_{10} \left( \frac{V_{\text{out}}}{V_{\text{in}}} \right) = 7.78 \times 10^8 \, \text{Hz}
\]

11.3. Determine the $-3 \, \text{dB}$ bandwidth of the circuits shown in Fig. 11.62. Assume $V_A = \infty$ but $\lambda > 0$. Neglect other capacitances.

![Figure 11.62 (c) and (d)]

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{\lambda R_1 C_s} \Rightarrow \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{\lambda R_1 C_s}
\]

\[
-3 \, \text{dB} = \frac{1}{\lambda R_1 C_s}
\]

\[
-3 \, \text{dB} = \frac{1}{\lambda R_1 C_s}
\]
11.4. Construct the Bode plot of $|V_{\text{out}}/V_{\text{in}}|$ for the stages depicted in Fig. 11.62.

11.9. Figure 11.63 illustrates a cascade of two identical CS stages. Neglecting channel-length modulation and other capacitances, construct the Bode plot of $|V_{\text{out}}/V_{\text{in}}|$. Note that $V_{\text{out}}/V_{\text{in}} = (V_x/V_m)(V_{\text{out}}/V_x)$. 
11.10. In Problem 11.9, derive the transfer function of the circuit, substitute \( s = j\omega \), and obtain an expression for \( |V_{\text{out}}/V_{\text{in}}| \). Determine the \(-3\) dB bandwidth of the circuit.

\[
\begin{align*}
|G(s)| &= \frac{j\omega R_0}{1 + j\omega R_0 C_L} \\
|H(s)| &= \frac{j\omega R_0}{1 + j\omega R_0 C_L} \\
\lambda > 0
\end{align*}
\]

Since \( \lambda > 0 \), we have an ideal current source, and the impedance looking from source to ground is \( \frac{1}{\omega C_L} \).

\[
\begin{align*}
V_{\text{out}} &= -j\omega V_{\text{in}} \left( \frac{1}{\omega C_L} \right) \\
H(s) &= -j\omega R_0 \left( \frac{1}{\omega C_L} \right) \\
|H(\omega)| &= \frac{j\omega R_0}{\sqrt{(\omega C_L)^2 + 1}} \\
\lambda \to 0, \ V_0 \to \infty \Rightarrow H(s) \to \frac{-j\omega R_0}{V_0 C_L} \\
H(s) &= -j\omega, \ \text{A pole at origin, thus} \\
&\text{operating as an ideal integrator.}
\end{align*}
\]
11.11. Due to a manufacturing error, a parasitic resistance $R_p$ has appeared in series with the source of $M_1$ in Fig. 11.64. Assuming $\lambda = 0$ and neglecting other capacitances, determine the input and output poles of the circuit.

$$\lambda = 0$$

To find input pole, let $V_{in} = 0$ and find the equivalent resistance and capacitance from node $X$ to ground.

$$R_X = \frac{R_S}{1 + \frac{1}{C_{in} f_m}}$$

$$\omega_{p_{in}} = \frac{1}{C_{in} \left[ \frac{1}{R_S} + \frac{1}{C_{in} f_m} \right]}$$

$$\omega_{p_{out}} = \frac{1}{R_o C_L}$$
11.14. Repeat Problem 11.12 for the CS stage depicted in Fig. 11.67.

\[ R_x = R_s, \quad R_{out} = R_0 \]

\[ C_x = C_m, \quad C_{out} = C_L \]

\[ G_{p,n} = \frac{1}{R_x C_m}, \quad G_{p,out} = \frac{1}{R_0 C_L} \]

11.16. Apply Miller’s theorem to resistor \( R_F \) in Fig. 11.68 and estimate the voltage gain of the circuit. Assume \( V_A = \infty \) and \( R_F \) is large enough to allow the approximation \( v_{out}/v_{in} = -g_m R_C \).

\[ V_{out} = \frac{-R_{out}}{\frac{1}{J_m} + \frac{R_x}{\beta + 1}} = \frac{-R_C}{\frac{1}{J_m} + \frac{R_F}{(1 + J_m R_C)}} \]
11.17. Repeat Problem 11.16 for the source follower in Fig. 11.69. Assume $\lambda = 0$ and $R_F$ is large enough to allow the approximation $v_{out}/v_x = R_L/(R_L + g_m^{-1})$.

\[ R_{out} = \frac{R_c}{1 - \frac{R_F}{R_c}} \]

\[ R_{out} = R_c / -\frac{R_F}{R_c} \]

\[ V_{out} = \frac{R_c}{R_c - R_F J_m R_c} \]

11.19. Using Miller’s theorem, estimate the input capacitance of the circuit depicted in Fig. 11.71. Assume $\lambda > 0$ but neglect other capacitances. What happens if $\lambda \to 0$?

\[ C_{in} = C_F(1 + J_m V_0) \text{, neglecting other } C_F \text{s.} \]

As $\lambda \to 0$, $V_0 \to \infty$, $C_{in} \to \infty$, $\omega \to 0$, $C_{in} \to \infty$, this bandwidth will $\to 0$. 

Figure 11.69

Figure 11.71
11.20. Repeat Problem 11.19 for the source follower shown in Fig. 11.72.

![Figure 11.72](image)

\[ V_{DD} \]
\[ C_{in} \]
\[ M_1 \]

\[ C_p \]

\[ V_{DD} \]
\[ C_{in} \]
\[ M_1 \]

\[ C_p \]

\[ \text{Figure 11.72} \]

\[ 20) \]
\[ V_{DD} \]
\[ \lambda > 0, \text{ DC gain} = \frac{V_o}{V_i} \]

\[ C_{in} = C_f\left(1 - \frac{1}{\lambda V_o}\right) \]

As \( \lambda \to 0, V_o \to \infty, \frac{1}{\lambda V_o} \to 0, C_{in} \to -\infty \)

When \( C \to \text{negative in value, we have} \)
\[ \text{inductive activity. So, right here, we have} \]
\[ \text{an effective infinite inductor.} \]

11.25. For the MOS circuits shown in Fig. 11.77, identify all of the transistor capacitances and determine which ones are in parallel.

![Diagrams of MOS circuits](image)

\[ C_{6_{52}, C_{6_{82}, C_{6_{81}}}} \text{ are in parallel} \]
\[ C_{6_{52}, C_{6_{82}}, C_{6_{81}}} \text{ are in parallel and grounded on both ends} \]
\[ C_{6_{81}} \text{ is grounded on both ends} \]

\[ C_{6_{51}, C_{6_{81}}, C_{6_{82}}} \text{ are in parallel} \]
\[ C_{6_{51}, C_{6_{81}}} \text{ are in parallel and grounded on both ends} \]
\[ C_{6_{82}} \text{ is grounded on both ends.} \]
\[\text{11.38. Assuming } \lambda > 0 \text{ and using Miller's theorem, determine the input and output poles of the stages depicted in Fig. 11.80.}\]

\[\begin{align*}
\text{a)} & \quad \frac{1}{R_s (C_{gs} + C_{gd} (1 + \frac{1}{Y_m}))} \\
\text{b)} & \quad \frac{1}{R_s (C_{gs} + C_{gd} (1 + \frac{1}{Y_m}))}
\end{align*}\]
11.39. In the CS stage of Fig. 11.29(a), $R_S = 200\ \Omega$, $R_D = 1\ \text{k}\Omega$, $I_D = 1\ \text{mA}$, $C_{GS} = 50\ \text{fF}$, $C_{GD} = 10\ \text{fF}$, $C_{DB} = 15\ \text{fF}$, and $V_{GS} - V_{TH} = 200\text{mV}$. Determine the poles of the circuit using (a) Miller’s approxima-
11.46. Determine the transfer function of the circuits shown in Fig. 11.86. Assume $\lambda = 0$ for $M_1$.

46)

a)

\[ V_{out} = \left( 3 - v_d \right) g_m \left[ \frac{1}{j_{m_2}} + \frac{1}{C_{G_S}} \right] \]

Note equation at $x, \quad \frac{V_x - V_m + V_m C_{G_S} - j_m(0-\omega) = 0}

\[ V_x \left( \frac{1}{R_S} + C_{G_S} + j_m \right) = \frac{V_m}{R_S} \Rightarrow V_x = \frac{V_m}{\left( 1 + R_S C_{G_S} + R_S j_m \right)} \]

Substitute in $V_x$ and solving for $V_{out}/V_{in} = \Rightarrow$

\[ V_{out} = \frac{g_m \left[ j_{m_2} \right]}{1 + R_S C_{G_S} + R_S j_m} \]

\[ \frac{V_m}{V_{out}} = \frac{j_m \left( 1/j_{m_2} \right)}{C_G (1/j_{m_2}) + \left( 1 + R_S C_{G_S} + R_S j_m \right)} \]

Similar to part a), with $j_m$ replaced by $\frac{1}{j_{m_2}}$ and different $C_G$

So

\[ \frac{V_{out}}{V_{in}} = \frac{j_m, V_{m_2}}{V_{in}} \left( C_G V_{m_2} + \frac{j_m}{R_S C_{G_S} + R_S j_m} \right) \]

Where $C_G = C_{GS} + C_{GS} + C_{GS} + C_{GS}$

\[ C_A = C_{GS} + C_{GS} \]
11.52. Using the results obtained in Problems 11.9 and 11.10, design the two-stage amplifier of Fig. 11.63 for a total voltage gain of 20 and a $-3$ dB bandwidth of 1 GHz. Assume each stage carries a bias current of 1 mA, $C_L = 50 \text{ fF}$, and $\mu_C C_{ox} = 100 \mu\text{A/V}^2$.

$V_{in} = \frac{J_m (1/J_m)}{(C_L (V_{th}) + L)(1 + R_o C_{ox} + R_i J_m)}$

where $C_L = C_{ox} + C_{th} + C_{g_user} + C_{g_bias}$

$C_{C} = C_{g_user} + C_{th}$

$C_{A} = C_{g_user} + C_{th}$

Bias Current: 1 mA (each stage)

$C_L = 50 \text{ fF}$

$M_n (\text{eff}) = 10 \text{ mA A/V}$, $A_v = 20$, $-3$ dB: 16 Hz

DC $J_{m, \text{in}}$: $\left(\frac{J_{m} R_o}{2}\right)^2 = 20$

$-3$ dB bandwidth: $0.1024$ (R/Ro) = 16 Hz

$C_{th} = 50 \text{ fF}$, $R_0 = 2000 \text{ fF}$

$J_{m, \text{in}} = 20 \Rightarrow J_{m} = 0.002183 = 2 I_o = V_{th} = 0.716 V$

$V_{th} = V_{th} = 0.716 V$

$g_m = \mu (C_{th} + (V_{th}) = \frac{V_{th}}{L} = \frac{J_{m}}{\mu (C_{th} (V_{th}))}$

$S_0 = R_0 = 2.05 k\Omega$, $C_L = 50 \text{ fF}$

$V_{th} = 0.716 V$, $W/L = 23.83$
11.57. An NMOS source follower must drive a load resistance of 100Ω with a voltage gain of 0.8. If $I_D = 1\ mA$, $\mu_C = 100\ \mu A/V^2$, $C_{ox} = 12\ fF/\mu m^2$, and $L = 0.18\ \mu m$, what is the minimum input capacitance that can be achieved? Assume $\lambda = 0$, $C_{GD} \approx 0$, $C_{SB} \approx 0$, and $C_{GS} = (2/3)WL/C_{ox}$.

\[ \begin{align*}
R_L &= 10\ \Omega, \quad I_o = 1mA \\
A_0 &= \frac{V_{in}}{V_{out}} = 0.8 \quad N_m C_{m} = 10\ \mu A/V^2 \\
L &= 0.18\ \mu m, \quad \lambda = 0, \quad C_{ox} = 12\ fF/\mu m \\
C_{SB} &= C_{GS} = (2/3)WL/C_{ox} \\
C_{m} &= 12 fF/\mu m \\
C_{id} &= C_{GS} + C_{GS}(0.2), \quad C_{in} = C_{ox}(0.2) = C_{wcm} \\
A_0 &= \frac{R_L}{R_L + 1/N_m} = 0.8, \quad \frac{1}{N_m} = 25 = \frac{V_{ss}}{2I_p} \\
V_{sh} &= 50\ mV, \quad I_o = 0.12 N_m C_{ox} (V_{th})^2 \Rightarrow I_o = 440 \\
C_{m,m} &= 0.2 C_{GS} = 0.2 \left(\frac{2}{3}\right) WL C_{ox} = 41.44 fF \\
on \Delta \quad C_{wcm} &= 41.45 fF
\end{align*} \]